What is Claimed is:

1. During the testing of the operation of processing unit, a system for identifying the occurrence of a new secondary code execution start point condition in the pipeline flattener, the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream;

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream; and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals resulting in periodic sync markers in the timing trace stream and in the program counter trace stream.

wherein the program counter trace apparatus is responsive to a new secondary code execution start point signal, the program counter trace apparatus generating a sync marker signal group identifying the occurrence of the new secondary code execution start point signal and relating the beginning of new secondary code execution start point to the timing trace stream and to the program code execution.

2. The system as recited in claim 1 wherein the marker signal group includes a program counter address, a timing index and a periodic sync ID.

3. The system as recited in claim 1 further comprising:

data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream, wherein the periodic signals are applied to the data trace apparatus resulting in periodic sync markers in the data trace stream; and

a host processing unit, the host processing unit responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstructing the processing activity of the processing unit from the trace streams.

4. The method for communicating an occurrence of a new secondary code execution start point signal from a target processor unit to a host processing unit after return from an original secondary code execution sequence, the method comprising:

generating a timing trace stream, a program counter trace stream, and data trace stream, and

in the program counter trace stream, including a program code start point sync marker signal group indicating an occurrence of a new secondary code execution

start point signal and relating the signal occurrence to the data trace stream and to the timing trace stream.

5. The method as recited in claim 4 further including:

including periodic sync markers in the timing trace stream and in the program counter trace stream; and

including in the new secondary code execution start point sync marker reference to a periodic sync marker.

6. In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, a new secondary code execution start point sync marker signal group in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a new secondary code execution start point signal;

indicia of the relationship of the occurrence of the new secondary code execution start point signal to the target processor clock; and

indicia of the relationship of the occurrence of the new secondary code execution start point signal to the target processor program execution.

7. In a target processing unit generating trace test signals for transfer to a host processing unit, a program counter trace generation apparatus comprising:

sync marker assembly apparatus, the sync marker assembly apparatus including:

a storage unit;

a decoder unit responsive to a new secondary code execution start point signal for storing an indicia of the new secondary code execution start point signal in the storage unit, the decoder unit generating a control signal;

a gate unit having a timing index, a periodic sync signal, and a program counter address, the gate unit storing the timing index, the periodic sync signal and the program counter address in the storage unit in response to the control signal; and

a FIFO unit, the storage unit transferring the stored signals to the FIFO unit in the form of a program code start point sync marker.

8. The program counter trace apparatus as recited in claim 7 responsive to a selected control signal for transferring the new secondary code execution start point sync marker in the FIFO unit to an output port of the target processor.

9. The program counter trace apparatus as recited in claim 8 wherein the apparatus can form a periodic sync marker in response to a periodic sync signal.

10. The program counter trace apparatus as recited in claim 9 wherein the new secondary code execution start point signal indicates the change from a first instruction code sequence to a second instruction code sequence exiting the pipeline flattener.

11. The program counter trace apparatus as recited in claim 10 wherein the first instruction code sequence is an original interrupt service routine code and the second instruction sequence is a new interrupt service routine.